MULTIMEDIA UNIVERSITY

STUDENT ID NO

MULTIMEDIA UNIVERSITY

FINAL EXAMINATION

TRIMESTER 2, 2015/2016

ECE4116 – DIGITAL COMPUTER DESIGN

(All Section / Groups)

10 MARCH 2016
2:30 P.M – 4:30 P.M.
(2 Hours)

INSTRUCTION TO STUDENT

1. This examination paper consists of SIX (6) pages with FOUR (4) questions only.
2. Answer ALL questions. All questions carry equal marks and the distribution of the marks for each question is given.
3. Please print all your answers in the Answer Booklet provided.

Question 1

(a) Figure Q1a shows the truth table of functions X and Y, which obtained from variables A, B, and C.

A	B	C	X	Y
0	0	0	0	1
0	0	1	1	0
0	1	0	1	0
0	1	1	0	0
1	0	0	0	1
1	0	1	0	0
1	1	0	1	0
1	1	1	0	1

Figure Q1a

(i) Write simplified Boolean expressions for functions X and Y. [6 marks]

(ii) Write a complete VHDL entity with inputs A, B, and C, and outputs X and Y to describe the functions. [4 marks]

(b) A sequential circuit has TWO (2) inputs, W_1 and W_2, and an output, Z. Figure Q1b shows the circuit's Finite State Machine (FSM) chart.

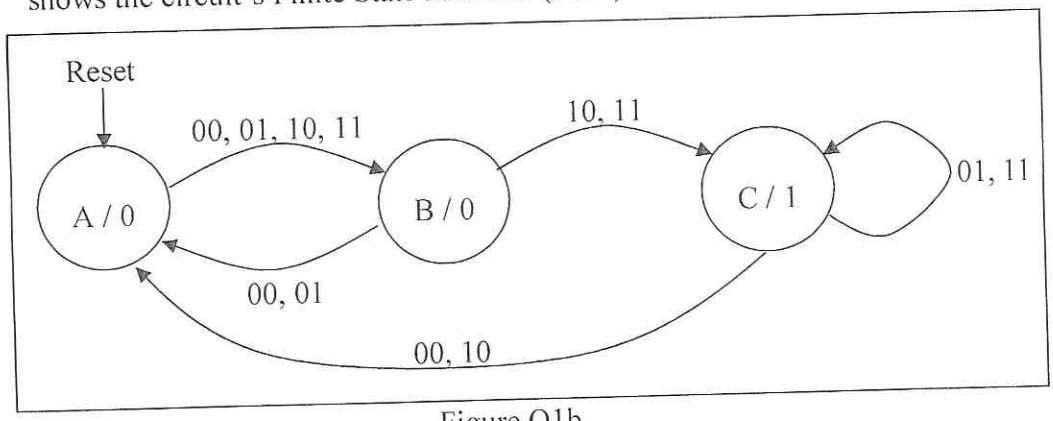

Figure Q1b

(i) Draw the Algorithmic State Machine (ASM) chart for the FSM in Figure Q1b. [5 marks]

(ii) Design the circuit using the one flip-flop per state technique. [10 marks]

Continued...

Question 2

(a) A digital system has TWO (2) registers, $R0$ and $R1$, and control signals $C1$, $C2$, and $C3$. The following register transfers must be implemented:

$$C1: R0 \leftarrow \overline{R1}$$
$$C2: R0 \leftarrow R1$$
$$C3: R0 \leftarrow 0$$

Draw the logic diagram to implement the register transfers. All the control signals are mutually-exclusive. When none are '1', no transfers occur.

[8 marks]

(b) A 3-state bus can have values of logic '0', '1' and Z-state.

(i) Describe the Z-state.

[2 marks]

(ii) Discuss the advantages of implementing 3-state buses with Z-outputs in a datapath.

[4 marks]

(c) A 512K×8 RAM chip uses coincident selection decoding.

(i) Compute the number of address lines of the RAM chip.

(2 marks)

(ii) Compute the number of inputs for the row decoder of the coincident selection scheme.

(3 marks)

(iii) Compute the number of inputs for the column decoder of the coincident selection scheme.

(3 marks)

(iv) Compare, in terms of total decoder outputs, between using a single decoder and using coincident selection decoding, for address decoding.

(3 marks)

Question 3

(a) The logic circuit of a hypothetical Arithmetic and Logic Unit (ALU) is to perform logic operations AND, OR, NOT, and XOR. Given n-bit data inputs A and B, output F, and selection signals S1 and S0,

(i) Write a function table to show how the selection signals can be used to control the logic operations to be performed on the data inputs to obtain output F.

[4 marks]

(ii) Design the logic circuit using multiplexers. Draw one stage (a single bit) of the circuit.

[5 marks]

(b) The instruction formats and partial list of instructions of a hypothetical computer are given in Figures Q3a and Q3b. Write the appropriate instruction to achieve each of the following operations. Subsequently, write the corresponding 16-bit binary code of the instruction.

i) Subtract the content of R5 from R6, store the result in R4.

(4 marks)

ii) Add decimal value 3 to R2, store the result in R1.

(4 marks)

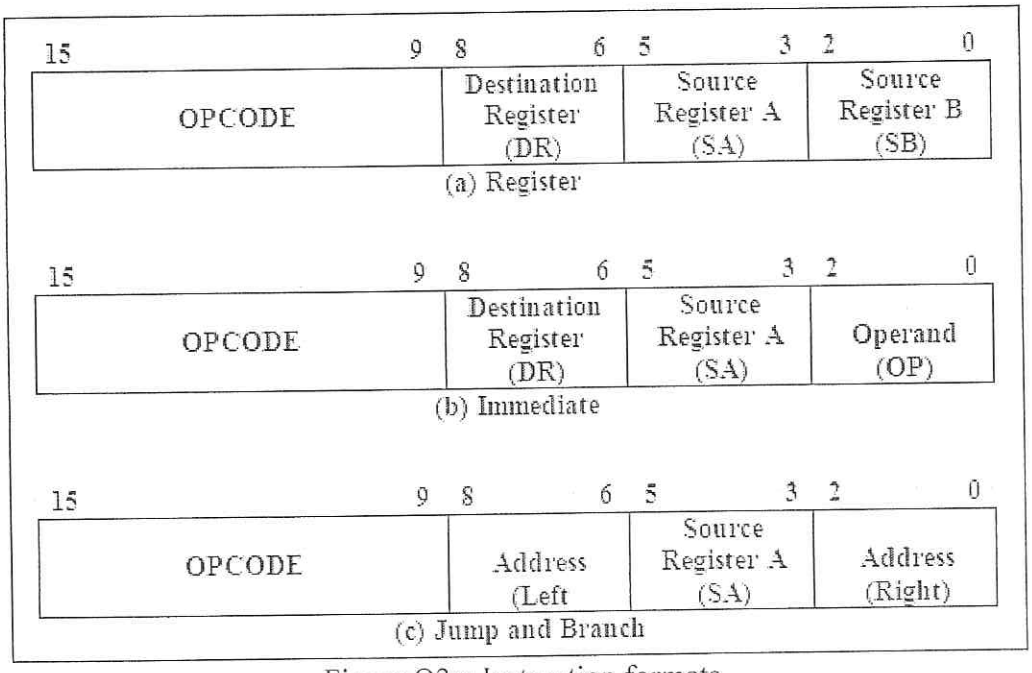

Figure Q3a: Instruction formats

Continued...

Operation	Symbolic Notation	Opcode	Action
Move A	MOVA	0000000	$R[DR] \leftarrow R[SA]$
Add	ADD	0000010	$R[DR] \leftarrow R[SA] + R[SB]$
Add Immediate	ADI	1000010	$R[DR] \leftarrow R[SA] + \text{zf } OP$
Subtract	SUB	0000101	$R[DR] \leftarrow R[SA] + \overline{R[SB]} + 1$
Load	LD	0010000	$R[DR] \leftarrow M[R[SA]]$
Load Immediate	LDI	1001100	$R[DR] \leftarrow \text{zf } OP$
Store	ST	0100000	$M[R[SA]] \leftarrow R[SB]$

Figure Q3b: Partial list of instructions

(c) A hypothetical computer has no general-purpose registers. Given

$$X = (A + B)/(C - D)$$

where A, B, C, D, and X are memory addresses, write a program to evaluate the expression for each of the following constraints. Use instructions MOV, ADD, SUB, MUL and DIV, and minimal number of temporary memory storage.

(i) Using only three-address instructions.

[4 marks]

(ii) Using only two-address instructions.

[4 marks]

Question 4

(a) A hypothetical RISC machine executes the following sequence of instructions in a typical 4-stage pipeline:

```
MOVA    R3, R8
SLT     R2, R4, R3
BZ      R2, 7
MOVA    R6, R10
```

(i) Draw the pipeline execution diagram to show the execution of the instructions. Subsequently, identify all hazards and specify the types.

[7 marks]

(ii) Describe the methods to resolve the hazards identified in part (i).

[6 marks]

Continued...

(b) The instruction formats and partial list of instructions of a hypothetical RISC machine with 32-bit words is given in Figures Q4a and Q4b. Consider the following instruction:

ANI R2 R5 1A35

i) The Instruction Register (IR) contains this instruction. Show the content of IR in hexadecimal value.

[4 marks]

ii) Given the content of $R5$ is **301A0FC7**. Compute the content of $R2$ at the end of the instruction execution cycle.

[4 marks]

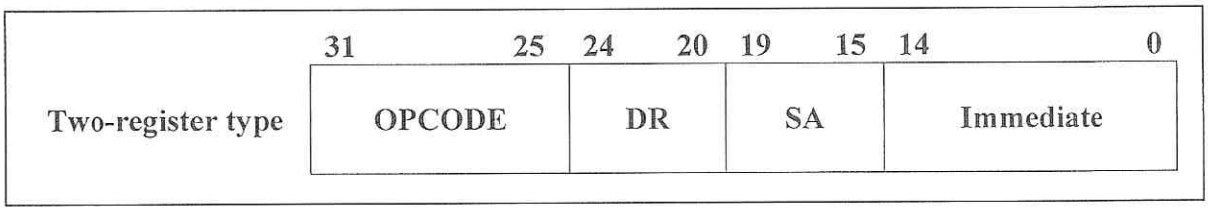

Figure Q4a: Instruction format

Operation	Symbolic Notation	Opcode	Action
AND Immediate	ANI	0101000	$R[DR] \leftarrow R[SA] \wedge (0 \parallel IM)$
OR Immediate	ORI	0101001	$R[DR] \leftarrow R[SA] \vee (0 \parallel IM)$
Exclusive-Or Immediate	XRI	0101010	$R[DR] \leftarrow R[SA] \oplus (0 \parallel IM)$

Figure Q4b: Partial list of Instructions

(c) Describe the characteristics of a CISC machine that make it unsuitable for the standard pipelining implementation.

[4 marks]

End of Paper